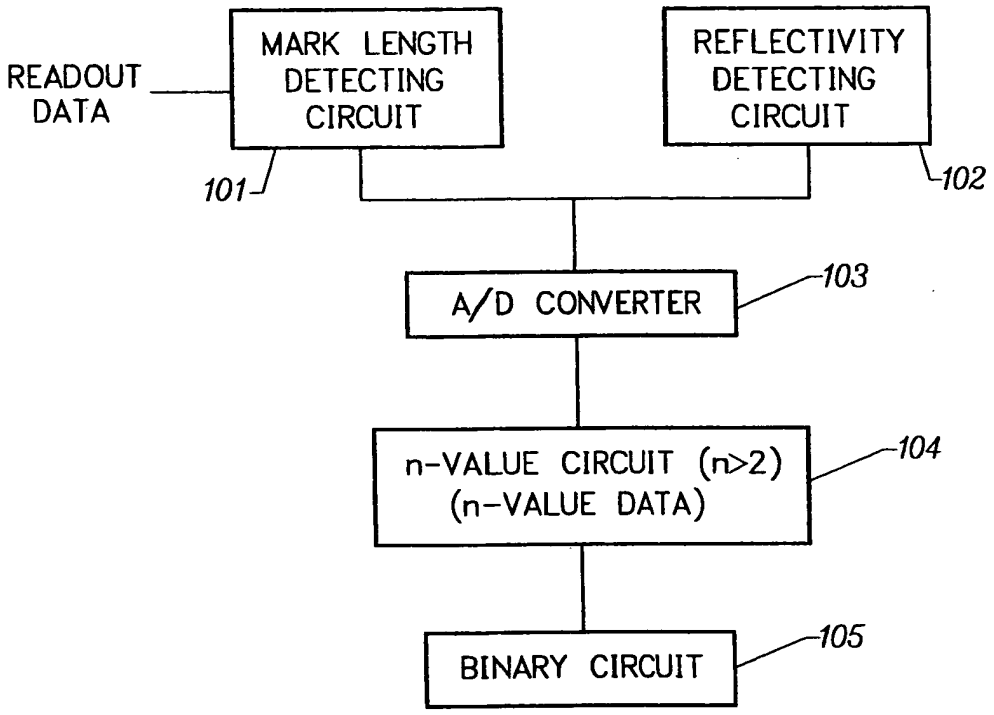


FIG. 1
(PRIOR ART)

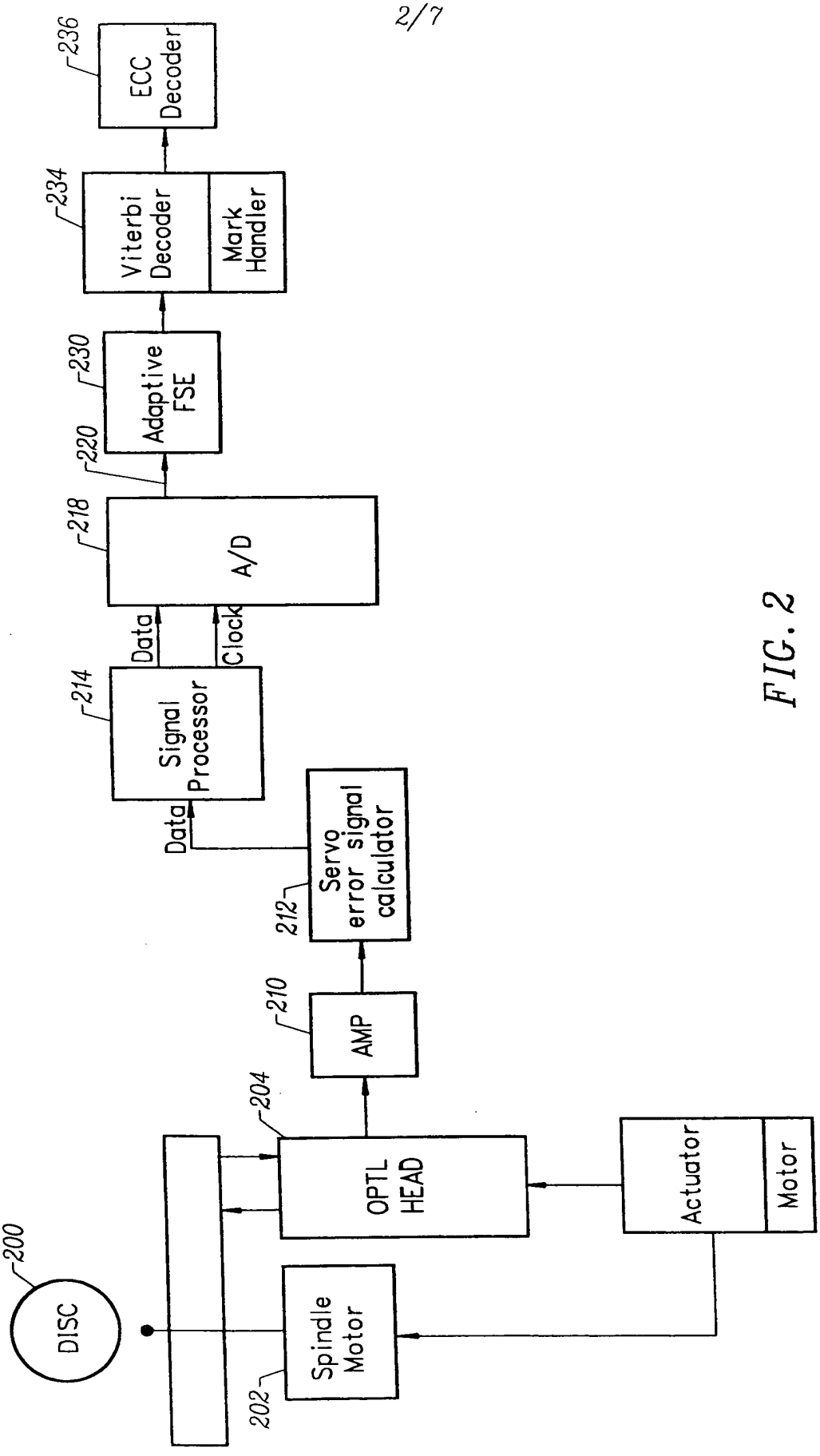

DISC
200
Spindle Motor
202
OPTL HEAD
204
Actuator
Motor
AMP
210
Servo error signal calculator
212
Signal Processor
214
Data
Clock
A/D
218
220
Adaptive FSE
230
Viterbi Decoder
Mark Handler
234
ECC Decoder
236

FIG. 2

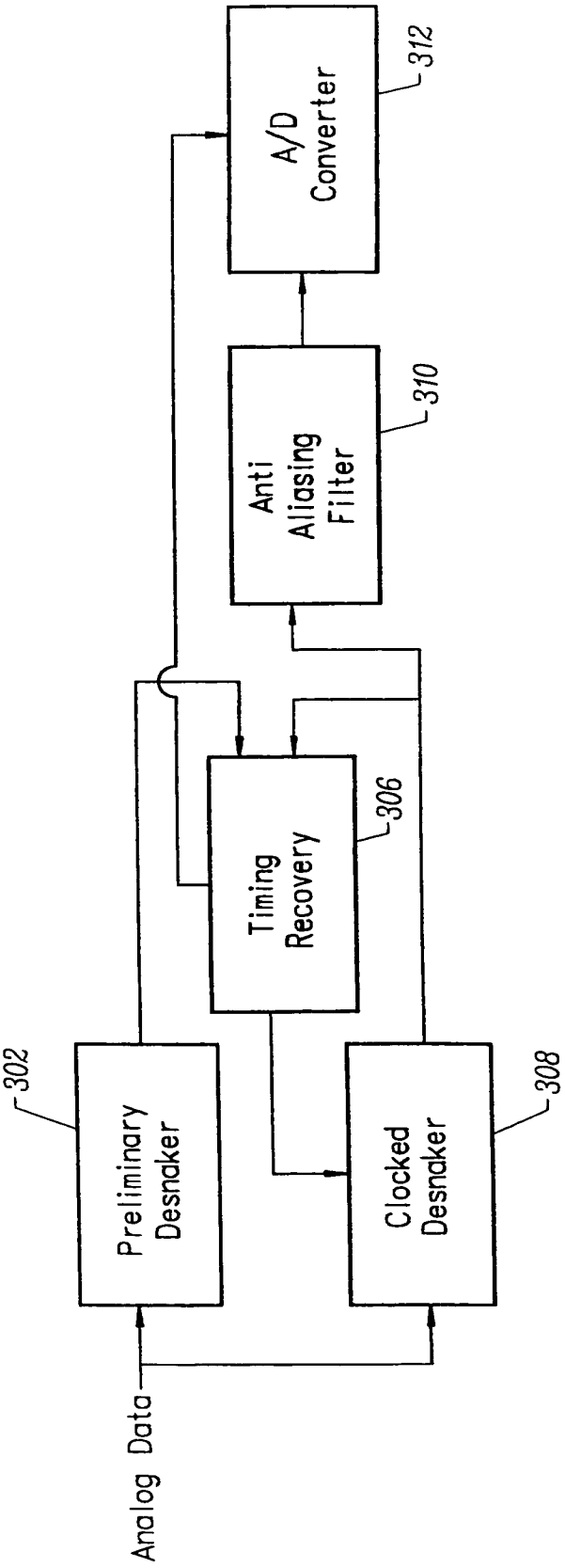

A/D Converter
312
Anti Aliasing Filter
310
Timing Recovery
306
Preliminary Desnaker
302
Clocked Desnaker
308
Analog Data

FIG. 3A

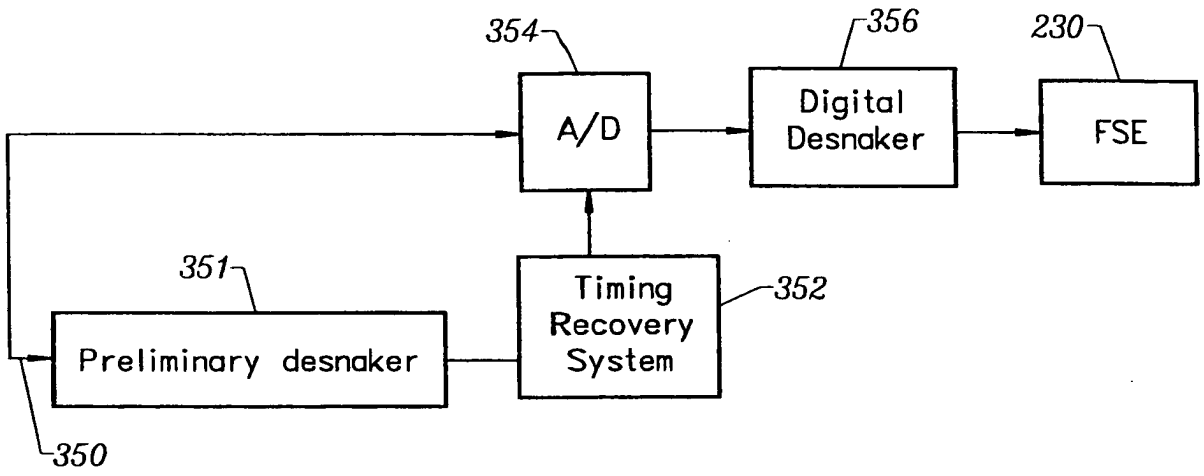

354
356
230
A/D
Digital Desnaker
FSE
351
Timing Recovery System
352
Preliminary desnaker
350

FIG. 3B

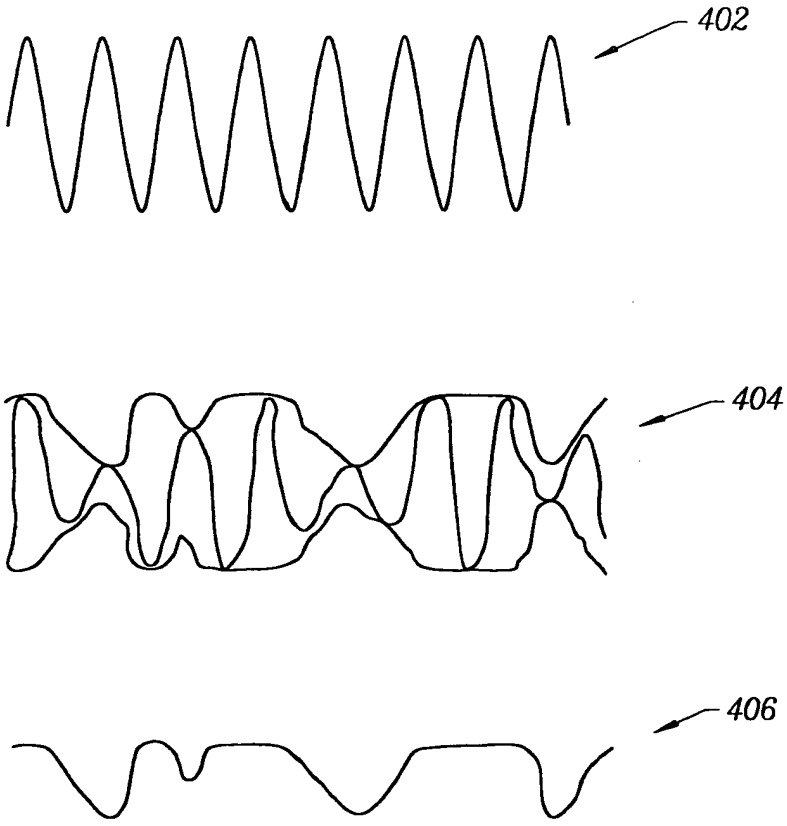


FIG. 4

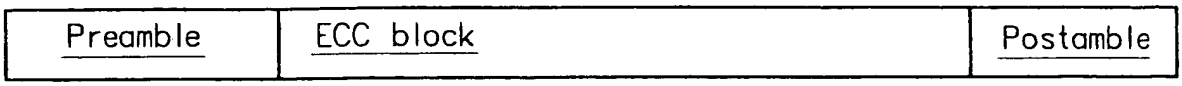


FIG. 5A

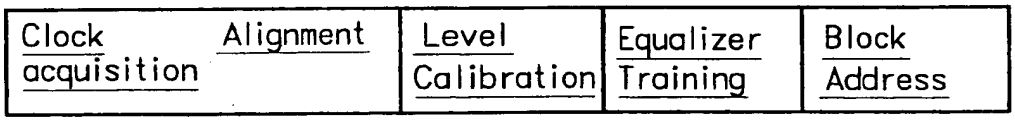


FIG. 5B

Preamble format

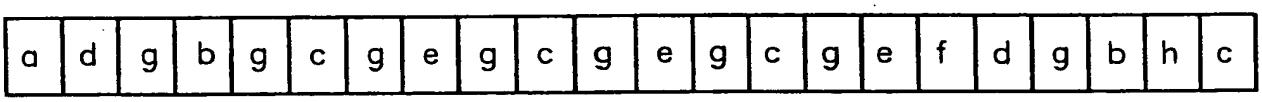
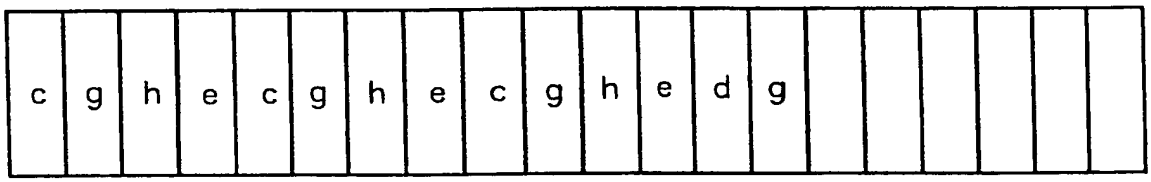


FIG. 5C

a address
b Erc data synch
c timing fields
d AGC
e DC
f ECC
g data
h trellis cleanup

Data block/ECC format

a d g b g c g e g c g e g c g e f d g b h c



c timing fields
g filler data
h trellis cleanup
e DC control
d AGC fields

Postamble format

c g h e c g h e c g h e d g

FIG. 5D

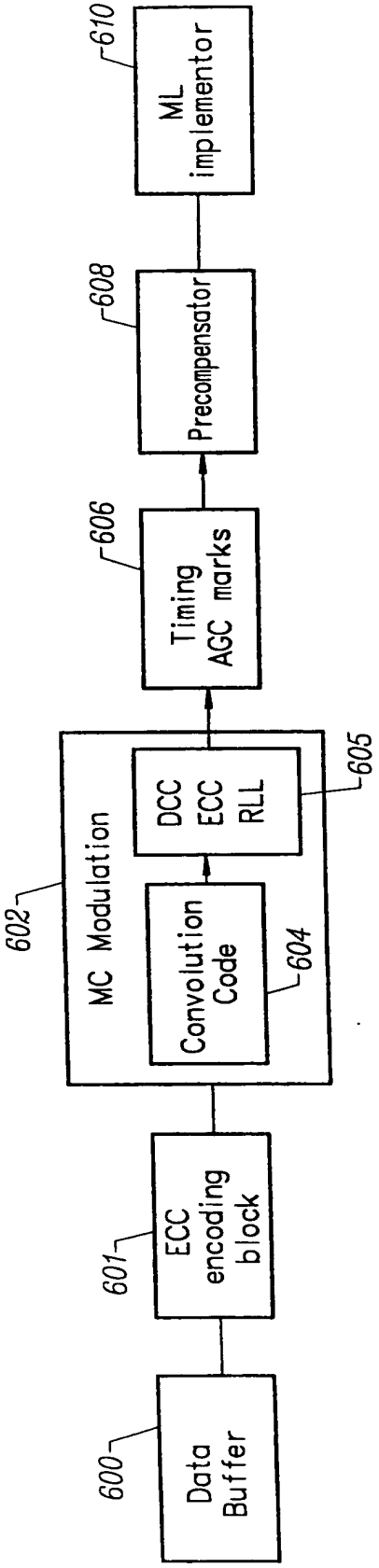

610
ML implementor
608
Precompensator
606
Timing AGC marks
602
MC Modulation
DCC ECC RLL
605
Convolution Code
604
601
ECC encoding block
600
Data Buffer

FIG. 6